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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/643,380	08/21/2000	Manoj Khare	42390.P9301	8768

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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,380	KHARE ET AL.	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/10/04 has been entered.

2. The applicant's amendment filed 6/10/04 has been considered. Claims 1-26 are pending in this Office Action.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al., U.S. Patent No. 6,085,263, hereinafter Sharma in view of Ebner et al., U.S. Patent No. 6,718,454, hereinafter Ebner.

As per claim 1, Sharma teaches the use of an apparatus comprising:

a prefetch engine to prefetch data from a distributed, coherent memory in response to a first transaction from an input/output bus directed to the distributed, coherent memory (e.g. abstract and col. 13, lines 20-42); and

an input/output coherent cache buffer to receive the prefetched data, the coherent cache buffer being coherent with the distributed, coherent memory and with other cache memories in a system including the input/output coherent cache buffer (e.g. abstract and col. 13, lines 20-42),

the prefetch engine further to prefetch data for the memory transactions from the I/O bus (abstract; figure 8, elements 810, 140). Sharma does not specifically show the use of speculatively prefetch data in association with a second input/output transaction if data has been prefetched for pending, memory-related transactions. Ebner shows the use of speculatively prefetch data in association with a second input/output transaction if data has been prefetched for pending, memory-related transactions (e.g. abstract; fig. 4; and col. 5, line 35 to col. 6, line 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ebner with Sharma because it would provide for a reduction in memory access time by predicting prefetch data ahead and avoid conflicting of multiple prefetch transactions, as taught by Ebner col. 1, lines 55-68 and col. 2, 45-68).

As per claim 2, Sharma teaches the use of the prefetch operation performed by the prefetch engine is a non-binding prefetch operation such that the prefetched data

received by the coherent cache buffer may be altered by a memory in the distributed coherent memory (e.g. col. 7, lines 20-23 and figure 9).

As per claim 3, Sharma teaches the use of the first transaction request is a memory read request and the prefetch engine issues a read request to prefetch data to be read from the distributed, coherent memory in response to the first transaction request (e.g. col. 5, lines 7-47).

As per claim 4, Sharma teaches the use of the first transaction request is a memory write request and the prefetch engine issues a request to prefetch ownership of a memory line in the distributed, coherent memory, the memory line being indicated by the first transaction request (e.g. col. 5, lines 18-21 and col. 7, lines 24-38).

As per claim 5, Sharma teaches the use of an input/output transaction request buffer to temporarily store transaction requests received from the input/output bus directed to the distributed, coherent memory (e.g. figure 2, elements 212 to 228 and figure 10, elements 812, 814).

As per claim 6, Sharma teaches the use of the prefetch engine prefetches data in response to transaction requests stored in the input/output transaction request buffer (e.g. abstract and col. 14, lines 9-37).

As per claim 7, Sharma teaches the use of the prefetch engine prefetches data in response to transaction requests stored in the input/output transaction request buffer regardless of the order in which the transaction requests were received from the input/output bus (e.g. abstract and col. 14, lines 9-37).

As per claim 8, Sharma teaches the use of a retire engine to retire input/output transaction requests stored in the transaction request buffer in program order after the transaction requests have been completed (e.g. abstract and col. 14, lines 9-37).

As per claim 9, Sharma teaches the use of the retire engine is further to check the input/output coherent cache buffer to determine whether data associated with an input/output transaction request to be retired is present in the input/output coherent cache buffer in a valid state (e.g. col. 14, line 61 to col. 15, line 6).

As per claim 10, Sharma teaches the use of coherency is maintained between the input/output coherent cache buffer and the distributed, coherent memory using a MESI protocol (e.g. col. 7, lines 24-40 and col. 8, lines 8-30).

As per claim 11, Sharma teaches a method comprising:

prefetching data in response to a first input/output transaction request received from an input/output bus and directed to a distributed, coherent memory (e.g. abstract and col. 13, lines 20-42);

prefetched data for pending memory –related input/output transactions (e.g., abstract);

temporarily storing the prefetched data(e.g. abstract and col. 13, lines 20-42); and

maintaining coherency between the prefetched data and data stored in the distributed, coherent memory and data stored in other cache memories (e.g. abstract and col. 13, lines 20-42; fig. 1, caches122-124; col. 7, lines 24-40 and col. 8, lines 8-30). Sharma does not specifically show the use of if data has been prefetch for pending memory transactions, speculatively prefetching data in anticipation of a need for the speculative prefetched data in association with a second input/output transaction. Ebner shows the use of if data has been prefetch for pending memory transactions, speculatively prefetching data in anticipation of a need for the speculative prefetched data in association with a second input/output transaction (e.g. abstract; fig. 4; and col. 5, line 35 to col. 6, line 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ebner with Sharma because it would provide for a reduction in memory access time by predicting prefetch data ahead and avoid conflicting of multiple prefetch transactions, as taught by Ebner col. 1, lines 55-68 and col. 2, 45-68).

As per claim 12, Sharma teaches buffering input/output transaction requests received from the input/output bus that are directed to the distributed, coherent memory (e.g., col. 8, lines 40-55 and col. 14, lines 10-37).

As per claim 13, Sharma teaches the use of prefetching data in response to second and third buffered input/output transactions wherein prefetching data in response to the first, second and third buffered input/output transactions may be performed in any order (e.g. abstract and col. 14, lines 9-60).

As per claims 14-15, Sharma teaches the use of retiring the buffered input/output transactions in the order in which they were issued by the input/output bus (e.g. abstract and col. 14, lines 9-37); the use of the checking the temporarily stored, prefetched data to determine whether valid data corresponding to the transaction request to be retired is temporarily stored (e.g. col. 14, line 61 to col. 15, line 6).

As per claims 16-18, Sharma teaches maintaining coherency using a MESI protocol (e.g. col. 7, lines 24-40 and col. 8, lines 8-30); prefetching including: issuing a request for the data in response to the first transaction request, and receiving the requested data (e.g. col. 5, lines 7-47); and prefetching data in response to a second input/output transaction request received from the i/o bus and directed to the distributed, coherent memory occurs between issuing the request and receiving the requested data (e.g. col. 5, lines 18-21 and col. 7, lines 24-38).

As per claim 19, it is rejected for similar reasons as stated above. Furthermore, Sharma teaches the use of a computer system comprising:

first and second processing nodes each including at least one processor and at least one caching agent (e.g. figure 1, elements 102-106);

a distributed coherent memory wherein portions of the distributed coherent memory are included within each of the first and second processing nodes (e.g. figure 1, elements 122-128 and col. 13, lines 30-40); and

an input/output node coupled to the first and second processing nodes (e.g. figure 1, element 800), the input/output node comprising:

a prefetch engine to prefetch data from a distributed, coherent memory in response to a first transaction from a first input/output bus directed to the distributed, coherent memory (e.g. abstract and col. 13, lines 20-42) and to prefetch data for pending memory-related transactions from the input/output bus (e.g., abstract and fig. 8, els. 810, 812, 872, 140); and

an input/output coherent cache buffer to receive the prefetched data, the coherent cache buffer being coherent with the distributed, coherent memory and the caching agents (e.g. abstract and col. 13, lines 20-42). Sharma does not specifically show the use of speculatively prefetch data after data has been prefetched for pending memory-related transactions in anticipation of a need for the speculative prefetched data in association with a second input/output transaction. Ebner shows the use of speculatively prefetch data after data has been prefetched for pending memory-related transactions in anticipation of a need for the speculative prefetched data in association

with a second input/output transaction (e.g. abstract; fig. 4; and col. 5, line 35 to col. 6, line 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ebner with Sharma because it would provide for a reduction in memory access time by predicting prefetch data ahead and avoid conflicting of multiple prefetch transactions, as taught by Ebner col. 1, lines 55-68 and col. 2, 45-68).

As per claim 20, Sharma teaches the use of a coherent system interconnect to couple each of the first and second processing nodes to the input/output node, the coherent system interconnect to communicate information to maintain coherency of the distributed, coherent memory and to maintain coherency between the input/output coherent cache buffer and the distributed, coherent memory (e.g. figure 1 and col. 7, line 10 to col. 8, line 40).

As per claim 21, Sharma teaches coherency is maintained using a MESI protocol (e.g. col. 7, lines 24-40 and col. 8, lines 8-30

As per claim 22, Sharma teaches the use of an interconnection network to communicate information between the first and second processing nodes and the input/output node (e.g. figures 1 and 4).

As per claim 23, Sharma teaches the use of an input/output bridge coupled between the first and second processing nodes and a plurality of input/output buses, the plurality of input/output buses including the first input/output bus, the input/output bridge including the prefetch engine and the input/output coherent cache buffer (e.g. figure 1, elements 102, 800 and 130, and figure 4).

As per claims 24, Sharma teaches the use of the input/output bridge comprising at least one i/o transaction requests received from the plurality of i/o buses that are directed to the distributed, coherent memory (e.g. figure 1, elements 102, 800 and 130, and figure 4; figure 2, elements 212 to 228 and figure 10, elements 812, 814).

As per claim 25, Sharma teaches the use of the prefetch engine prefetches data in response to transaction requests stored in the input/output transaction request buffer regardless of the order in which the transaction requests are stored (e.g. abstract and col. 14, lines 9-37).

As per claim 26, Sharma teaches wherein the i/o bridge further comprising: a retire engine to check the input/output coherent cache buffer for valid data corresponding to a transaction request to be retired (e.g. col. 14, line 61 to col. 15, line 6) and the retire engine to retire transaction requests stored in the i/o transaction request buffer in program order (e.g. abstract and col. 14, lines 9-37).

5. Applicant's remarks filed 6/10/04 have been considered, but are moot in view of the new grounds of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday from 8:45 a.m. to 5:15 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran
11/24/04